	Source Unit	Info Type	~IACK	~IRQ	~RESET	~BUSY	~WR	~RD	Address	Data	I	O	N	Z	C	Inst	clk_alu_acc	clk_alu_tmp	~ena_alu_tbuf	clk_status_i	clk_status_o	clk_status_n	clk_status_z	clk_status_c	~set_im	~clr_im	sel_status_2_1	~ena_status_tbuf	clk_addr_pc_ms	clk_addr_pc_ls	clk_addr_tpca_ms	clk_addr_tpca_ls	clk_addr_tpcb_ms	clk_addr_tpcb_ls	clk_addr_sp_ms	clk_addr_sp_ls	clk_addr_iv_ms	clk_addr_iv_ls	clk_addr_x_ms	clk_addr_x_ls	clk_addr_latch	sel_addr_2_1_in	sel_addr_2_1_out	(2) sel_addr_5_1	(1) sel_addr_5_1	(0) sel_addr_5_1	(2) sel_addr_6_1	(1) sel_addr_6_1	(0) sel_addr_6_1	~ena_addr_tbuf_ms	~ena_addr_tbuf_ls
C	INITIALIZATION (Set cabinet into a known-good condition)																																																			
C	The first packet (which - in the real world - will be generated by the control unit) simply places the ~RESET signal in its inactive state.																																																		
T	00	20	1	1	1	1	1	1	0000	00	0	0	0	0	0	00	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C	A ROM cabinet transmits a byte of data ($00) from address $0000. No response is expected.																																																		
T	05	22	1	1	1	1	1	1	0000	00	0	0	0	0	0	00	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C	The control cabinet selects the data inputs in the status cabinet. No response expected.																																																		
T	00	20	1	1	1	1	1	1	0000	00	0	0	0	0	0	00	0	0	1	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C	The control cabinet activates all the status flag clocks. A response is expected.																																																		
T	00	20	1	1	1	0	1	1	0000	00	0	0	0	0	0	00	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C	The status logic returns the current status flags. Also ~BUSY is returned to its inactive state,																																																		
R	02	24	1	1	1	1	1	1	0000	00	0	0	0	0	0	00	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C	The control logic deactivates the clocks and the mux. No response is expected.																																																		
T	00	20	1	1	1	1	1	1	0000	00	0	0	0	0	0	00	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C																																																		
C	TEST #1: SET and CLEAR THE I (INTERRUPT MASK) FLAG																																																		
C	The control logic sets the ~set_im signal to its active state. A response is expected so ~BUSY is made active also.																																																		
T	00	28	1	1	1	0	1	1	0000	00	0	0	0	0	0	00	0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C	The status logic returns the current status flags. Also ~BUSY is returned to its inactive state,																																																		
R	02	24	1	1	1	1	1	1	0000	00	1	0	0	0	0	00	0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C	The control logic returns the ~set_im signal to its inactive state. No response is expected so ~BUSY is left inactive.																																																		
T	00	08	1	1	1	1	1	1	0000	00	1	0	0	0	0	00	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C	The control logic sets the ~clr_im signal to its active state. A response is expected so ~BUSY is made active also.																																																		
T	00	28	1	1	1	0	1	1	0000	00	1	0	0	0	0	00	0	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C	The status logic returns the current status flags. Also ~BUSY is returned to its inactive state,																																																		
R	02	24	1	1	1	1	1	1	0000	00	0	0	0	0	0	00	0	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C	The control logic returns the ~clr_im signal to its inactive state. No response is expected so ~BUSY is left inactive.																																																		
T	00	08	1	1	1	1	1	1	0000	00	0	0	0	0	0	00	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C																																																		
C	TEST #2: SET THE O, N, Z, AND C FLAGS ONE AFTER THE OTHER																																																		
C	The ALU logic sets the O flag. No response is expected.																																																		
T	01	24	1	1	1	1	1	1	0000	00	0	1	0	0	0	00	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C	The control logic clocks the O, N, Z, C flags. A response is expected.																																																		
T	00	20	1	1	1	0	1	1	0000	00	0	0	0	0	0	00	0	0	1	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C	The status logic returns the current status flags. Also ~BUSY is returned to its inactive state,																																																		
R	02	24	1	1	1	1	1	1	0000	00	0	1	0	0	0	00	0	0	1	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C	The control logic deactivates the clocks. No response is expected.																																																		
T	00	20	1	1	1	1	1	1	0000	00	0	1	0	0	0	00	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C	The ALU logic clears O and sets N. No response is expected.																																																		
T	01	24	1	1	1	1	1	1	0000	00	0	0	1	0	0	00	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C	The control logic clocks only the N, Z, C flags. A response is expected.																																																		
T	00	20	1	1	1	0	1	1	0000	00	0	1	0	0	0	00	0	0	1	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C	The status logic returns the current status flags. Also ~BUSY is returned to its inactive state,																																																		
R	02	24	1	1	1	1	1	1	0000	00	0	1	1	0	0	00	0	0	1	0	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C	The control logic deactivates the clocks. No response is expected.																																																		
T	00	20	1	1	1	1	1	1	0000	00	0	1	1	0	0	00	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C	The ALU logic clears N and sets Z. No response is expected.																																																		
T	01	24	1	1	1	1	1	1	0000	00	0	0	0	1	0	00	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C	The control logic clocks only the Z and C flags. A response is expected.																																																		
T	00	20	1	1	1	0	1	1	0000	00	0	1	1	0	0	00	0	0	1	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
C	The status logic returns the current status flags. Also ~BUSY is returned to its inactive state,																																																		

R 02 24 1 1 1 1 1 1 0000 00 0 1 1 1 0 00 0 0 1 0 0 0 1 1 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1
C The control logic deactivates the clocks. No response is expected.
T 00 20 1 1 1 1 1 1 0000 00 0 1 1 1 0 00 0 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1
C The ALU logic clears Z and sets C. No response is expected.
T 01 24 1 1 1 1 1 1 0000 00 0 0 0 0 1 00 0 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1
C The control logic clocks only the C flag. A response is expected.
T 00 20 1 1 1 0 1 1 0000 00 0 1 1 1 0 00 0 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1
C The status logic returns the current status flags. Also ~BUSY is returned to its inactive state,
R 02 24 1 1 1 1 1 1 0000 00 0 1 1 1 1 00 0 0 1 0 0 0 0 1 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1
C The control logic deactivates the Z clock. No response is expected.
T 00 20 1 1 1 1 1 1 0000 00 0 1 1 1 1 00 0 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1
C
C TEST #3: PRETEND TO DO A POPSR (Not the full thing)
C A RAM cabinet transmits a byte of data from address $EFFF. No response is expected.
T 05 22 1 1 1 1 1 1 EFFF F5 0 1 1 1 1 00 0 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1
C The control cabinet selects the data inputs in the status cabinet. No response expected.
T 00 20 1 1 1 1 1 1 EFFF F5 0 1 1 1 1 00 0 0 1 0 0 0 0 0 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1
C The control cabinet activates all the status flag clocks. A response is expected.
T 00 20 1 1 1 0 1 1 EFFF F5 0 1 1 1 1 00 0 0 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1
C The status logic returns the current status flags. Also ~BUSY is returned to its inactive state,
R 02 24 1 1 1 1 1 1 EFFF F5 1 0 1 0 1 00 0 0 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1
C The control logic deactivates the clocks and the mux. No response is expected.
T 00 20 1 1 1 1 1 1 EFFF F5 1 0 1 0 1 00 0 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1
C
C TEST #4: PRETEND TO DO A PUSHSR (Not the full thing)
C A RAM cabinet transmits a byte of data from address $ABCD. No response is expected.
T 05 22 1 1 1 1 1 1 ABCD AA 1 0 1 0 1 00 0 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1
C The control cabinet activates the status logic's tri-state enable. A response is expected.
T 00 20 1 1 1 0 1 1 ABCD AA 1 0 1 0 1 00 0 0 1 0 0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1
C The status logic returns the status flags on the data bus. Also ~BUSY is returned to its inactive state,
R 02 22 1 1 1 1 1 1 ABCD 15 1 0 1 0 1 00 0 0 1 0 0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1
C The control logic deactivates the status logic's tri-state enable. No response is expected.
T 00 20 1 1 1 1 1 1 ABCD 15 1 0 1 0 1 00 0 0 1 0 0 0 0 0 1 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1